Available online at www.sciencedirect.com
ScienceDirect
Sensors and Actuators A 138 (2007) 112–119
SENSORS AND ACTUATORS A PHYSICAL
www.elsevier.com/locate/sna

ASIC front-end interface with frequency and duty cycle output for resistive-bridge sensors

V. Ferrari *, A. Ghisla, Zs. Kovács Vajna, D. Marioli, A. Taroni

University of Brescia, Department of Electronics for Automation and INFM, Via Branze 38, 25123 Brescia, Italy

Received 20 June 2006; received in revised form 17 April 2007; accepted 20 April 2007
Available online 27 April 2007

Abstract

An application specific integrated circuit (ASIC) front-end interface in 0.7-μm CMOS for resistive-bridge sensors is proposed. The circuit is based on a relaxation oscillator where the frequency of the rectangular-wave output is related to the fractional bridge unbalance, and the duty cycle depends on the overall bridge resistance, which typically is related to temperature. In this way, two independent pieces of information are simultaneously and cost-effectively carried on the same output signal. The bridge is driven at constant current, this avoids accuracy degradation with remotely placed sensors and enables a first-order thermal compensation for piezoresistive semiconductor sensors. The circuit has been characterized by means of a 1-kΩ reference bridge showing frequency and duty cycle sensitivities of 60.4 Hz/(1000 ppm) and 0.276%/(mΩ/Ω), respectively, at a central frequency of about 6.4 kHz. The circuit has also been tested with a piezoresistive SiC sensor operated at temperatures up to 150 °C, showing results in agreement with theoretical predictions.

Keywords: Resistive-bridge sensor; Resistance-controlled oscillator; Sensor interface

1. Introduction

Resistive sensors are widely used in measurement and control systems. There are different technologies for the realization of resistive sensors and a wide diversity of measurands and applications exist where the sensitive elements can be arranged in single-element, differential or bridge configurations. The large diffusion of resistive sensors demands for a continuous improvement of electronic interfaces to fully exploit their potential. Recent examples are given for instance in Refs. [1–4], where resistive-sensor interfaces are presented either in the form of discrete or integrated circuits. Among the signal conditioning strategies, sensor interfaces in which either frequency, period, pulse width or duty cycle modulation is used for output transmission offer advantages compared to voltage- or current-output circuits [4–8]. Signal conversion into the frequency–time domain improves noise immunity and simplifies interfacing to digital systems, without communication protocols required. Moreover, the sensor readout can be accomplished with counting procedures that allow high resolution provided that measurement time is chosen appropriately. Sensors with output in the frequency–time domain are often referred to as quasi-digital. Measuring techniques [9,10] and devices [11] for the output readout of quasi-digital sensors have been developed, in particular for smart-sensor applications. A circuit interface for resistive-bridge sensor, based on a relaxation oscillator in which both the frequency and duty cycle of the output signal are independently related to two separate sensor readings, was previously proposed [12,13]. Such designs allow conveying in the same output signal, two independent pieces of information coming from the sensor. The first information is the primary measurement, and the second information can be related to the sensor temperature and then used, for instance, for thermal compensation algorithms. In Ref. [12] the bridge is driven by a square-wave voltage thereby reducing the effect of offset and drift of the input amplifier. The temperature is measured by an independent sensor placed near the bridge. In Ref. [13] the bridge is excited by a DC current to reduce the effect of stray and cable capacitances whereas the bridge unbalance voltage is switched at the amplifier input. The temperature of the sensor is determined by measuring the sensor bridge resistance itself. Furthermore, the DC current excitation makes the con-

* Corresponding author. Tel.: +39 030 3715444; fax: +39 030 380014.
E-mail address: vittorio.ferrari@unibs.it (V. Ferrari).

0924-4247/$ – see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2007.04.060

figuration unaffected by lead wire resistances, and enables a first-order thermal compensation in hardware with piezoresistive semiconductor sensors.

In this work, an ASIC is presented that has been designed based on the concept first proposed in Ref. [13]. The ASIC is highly versatile and offers a number of significant improvements inherent in the IC technology, such as a higher noise immunity and a reduction of stray capacitances that allows to reduce power consumption and to increase performances.

2. Circuit description

The ASIC interface has been manufactured in the Alcatel 0.7-μm standard CMOS technology as a service offered by the Europractice consortium. Fig. 1 shows a picture of the die that was mounted in a 28-pin dual-in-line ceramic package.

The overall circuit diagram, the expanded view of the current generators, and the relevant signals are shown in Fig. 2(a)–(c). The sensor bridge is connected through five wires whose respective resistances are denoted by R_{W1}–R_{W5}. We first assume that the sensor bridge is placed close to the ASIC, so that R_{W1}–R_{W5} are negligible.

A multiple-output current generator is formed by the matched PMOS transistors M1–M5, and the OpAmp A2 with biasing resistors. M5 and M4 output two identical currents I_B, one of which is used to excite the sensor bridge, while the other flows into an external reference resistor R_{bo}. The currents I_B are multiple by a factor $M = 8$ of the reference current I_{ref}, which can be set by the external resistor R_{ref} through the expression $I_{ref} = V_{DD}/(2R_{ref})$. The bridge output voltage V_U is proportional to the bridge resistive unbalance. The voltage V_E across the bridge is proportional to the overall bridge resistance $R_B = (R_1 + R_2)||(R_3 + R_4)$, which in turn is related to the sensor operating temperature. Therefore, the voltage V_B across the M5 and M4 outputs of the current generator provides an indirect measurement of sensor temperature referred to an offset set by R_{bo}.

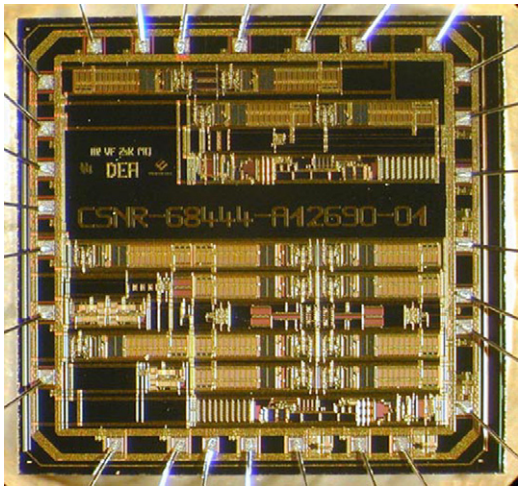


Fig. 1. Picture of the ASIC chip.

The voltages V_U and V_B are periodically switched in polarity by means of the switch pairs SW1–SW2 and SW3–SW4, and amplified by the differential amplifiers DA1 and DA2. The switching frequency is determined by the integration time on the external capacitor C_0 of the algebraic sum of the current I_γ, proportional to the bridge unbalance voltage V_U, and the offset current I_0 also produced by the multiple-output current generator. The current I_0 is switched in polarity by turning on and off the current mirror formed by the NMOS transistors M6 and M7 and the OpAmp A3 under the control of the switching transistors M8 and M9. Upward and downward integration intervals of $(I_\gamma \pm I_0)$ cyclically repeat with the integrator output V_1 being limited between the threshold voltages V_{TH} and V_{TL} of the window comparator C1–C2.

In addition, by means of the comparator C3, the integrator output V_1 is compared to the square wave V_T coming from the polarity switching of V_B. The resultant signal V_2 is phase shifted with respect to the driving signals V_{SW} by an amount dependent on V_B. The rectangular-wave output V_{out} is obtained by the EX-OR of V_2 and V_{SW}. Therefore, V_{out} carries information on V_U in its frequency f, and on V_B in its duty cycle dc.

If now finite values of the resistors R_{W1}–R_{W5} are assumed caused by a remotely placed bridge, the following considerations can be made.

Due to the high input impedance of DA1 and DA2, R_{W2} and R_{W3} have no influence in either V_U or V_B because there is no current flow in them.

Since the sensor bridge is driven at constant current, the series resistors R_{W1} and R_{W5} do not modify the voltage V_E developed across the bridge. In addition, R_{W4} does not influence V_E. Therefore, the bridge output voltage V_U does not depend on any wire resistance.

In the measurement of the voltage V_B the three-wire connection of the bridge allows the compensation of the voltage drops across the connection resistors R_{W1} and R_{W4}, assumed to be equal, whereas the voltage across R_{W5} plays no role. In fact, the voltage V_B results $V_B = (R_{w1}I_B + R_BI_B) - (R_{bo}I_B + R_{W4}I_B) = (R_B - R_{bo})I_B$. Therefore, the voltage V_B is also not influenced by any wire resistance.

Therefore, the adopted configuration is insensitive to wire resistances and preserves accuracy with remote sensors.

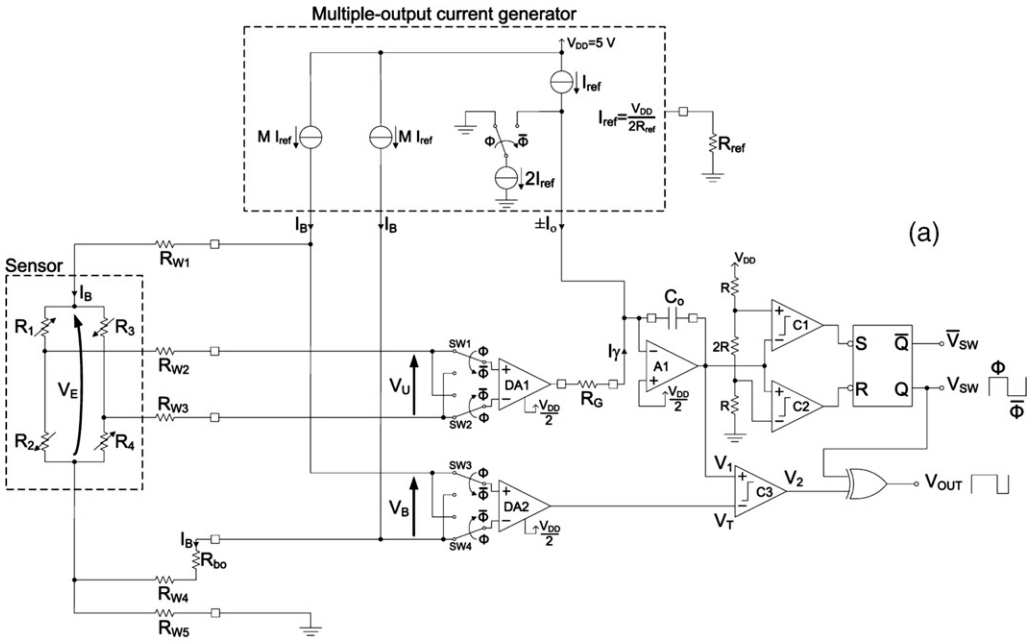
Summarizing, the expression of the output frequency f defined as $1/T$ in Fig. 2(c), is given by

$$f = f_0\left(1 + MG_1\frac{R_B}{R_G}\gamma\right) \tag{1}$$

where $M = 8$ is the current ratio between the mirrored current I_B and the reference current I_{ref}, $G_1 = 51$ the voltage gain of DA1, $f_0 = 1/(R_{ref}C_0)$ is the central frequency. The nondimensional term $\gamma = [R_2/(R_1 + R_2) - R_4/(R_3 + R_4)] = V_U/V_E$, where V_E is the voltage across the bridge, denotes the fractional bridge unbalance.

The expression of the duty cycle dc, defined as T_H/T in Fig. 2(c), is given by

$$dc = \frac{1}{2}\left(1 + 2\frac{\Delta R_B}{R_{bo}}\frac{MG_2R_{bo}}{R_{ref}}\right) \tag{2}$$



$$f = \frac{1}{T}$$

$$dc = \frac{T_H}{T}$$

Fig. 2. Schematic diagram of the ASIC interface where squared dots represent connections to external components (a); schematic of the current generator block (b); waveforms of relevant signals (c).

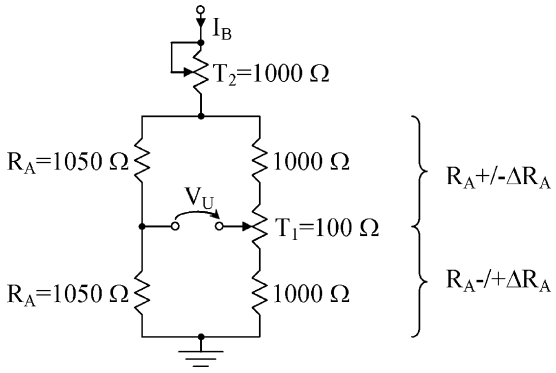


Fig. 3. Reference bridge configuration.

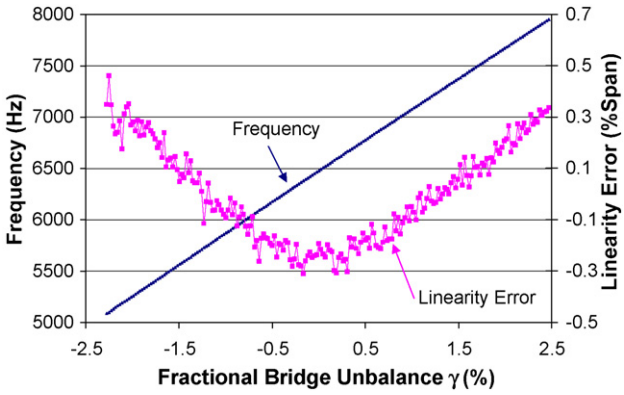


Fig. 4. Measured output frequency vs. fractional bridge unbalance.

where $G_2 = 13.8$ is the voltage gain of DA2 and $\Delta R_B/R_{bo}$ is the fractional variation of the overall bridge resistance with respect to the reference value $R_B = R_{bo}$.

The only components external to the ASIC are C_0 and R_{ref} which set the central frequency f_0, R_G which sets the gain for γ, and R_{bo}.

Both expressions (1) and (2) are linear with γ and $\Delta R_B/R_{bo}$, respectively, without mutual dependence. In this way, two independent measurement values are simultaneously carried on the same output signal with no cable extra-cost.

It can be observed that the EX-OR stage provides a frequency-doubling action, therefore the oscillator core works at half the output frequency. For a given output frequency, this reduces the linearity degradation due to the switching delays, which is a typical limitation for configurations based on relaxation oscillators [8,13].

The DC current excitation of the bridge, besides avoiding the influence of wire resistances, also reduces the effect of stray capacitances because they are not cyclically charged and discharged, as it would occur in switched-polarity bridge excitation [7,8]. The polarity switching of voltages V_U and V_B introduces a chopper action that mitigates the effect of the offset voltage and low-frequency noise of the input amplifiers [13], thereby avoiding the requirements for low-offset and high DC-precision amplifiers.

The ratiometric design topology advantageously gives first-order independence from fluctuations of power supply voltage V_{DD}, since fluctuations of V_{DD} affect both the thresholds of the comparator and the integration current of the same factor.

3. ASIC characterization

The ASIC mounted on a breadboard with the auxiliary external components ($C_0 = 2.2$ nF, $R_{ref} = 67.8$ kΩ, $R_G = 46.7$ kΩ) was tested with a reference 1-kΩ bridge. The bridge is shown in Fig. 3, and is made by precision resistors and a multiturn wire potentiometer $T_1 = 100$ Ω arranged in a half-bridge configuration. In this case the fractional unbalance γ is equal to $\Delta R_A/(2R_A)$ where R_A is the resistance of a single arm. The overall bridge resistance R_B could be changed by means of a second multiturn potentiometer $T_2 = 1$ kΩ placed in series with the bridge. The fractional bridge unbalance γ, and the fractional variation of the overall bridge resistance $\Delta R_B/R_{bo}$ could be set with a resolution of 48 ppm and 0.64 mΩ/Ω, respectively. The frequency and duty cycle of the output waveform were measured by means of a computer-based acquisition system connected to a HP 53132 frequency counter. The current consumption of the circuit is about 14 mA at $V_{DD} = 5$ V.

The preliminary check of the signals of Fig. 2(c) showed that the window width $\Delta V = V_{TH} - V_{TL}$ of the comparator C1–C2 at $V_{DD} = 5$ V was 2.61 V, as opposed to the nominal value $\Delta V = V_{DD}/2 = 2.5$ V. As a consequence, the corrected expression of the central frequency becomes $f_0 = (2.5/2.61)/C_0R_{ref}$. Using the above-cited values of C_0 and R_{ref} results in an expected value of $f_0 = 6.4$ kHz.

Fig. 4 shows the measured shift of the output frequency f versus the fractional bridge unbalance γ. The measurements were taken with the potentiometer T_2 set to 0 and the reference value R_{bo} set to 1055 Ω.

The central frequency is about 6.4 kHz, as expected. The frequency sensitivity $(f - f_0)/\gamma$ is 60.4 Hz/(1000 ppm) in good agreement with the theoretical sensitivity of 59.3 Hz/(1000 ppm). The best-fit line nonlinearity results smaller than ±0.4% of the span. The "U" shaped trend of the linearity error is typical of relaxation oscillators, being caused by the parasitic delay times in the loop [8,12], but in the present case a significant quantitative improvement is obtained.

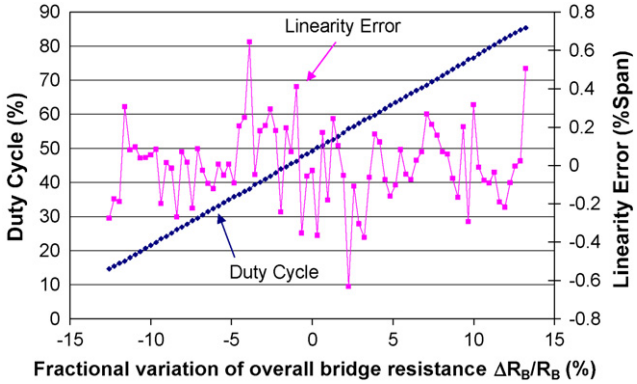


Fig. 5. Measured output duty cycle vs. fractional variation of overall bridge resistance.

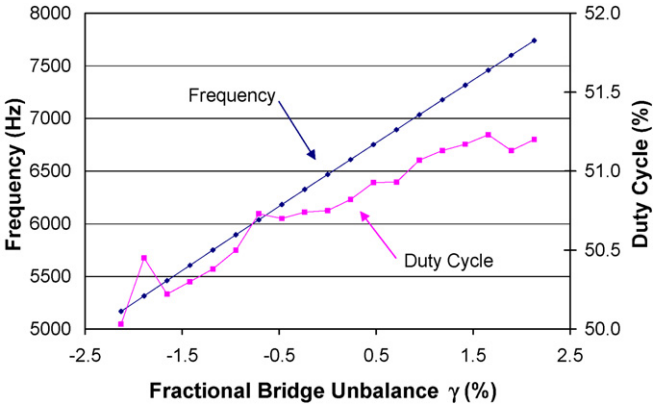


Fig. 6. Measured frequency and duty cycle vs. fractional bridge unbalance at constant bridge resistance.

Fig. 5 shows the measured output duty cycle *dc* versus the fractional variation of the overall bridge resistance $\Delta R_B/R_{bo}$. In this case, the potentiometer T_2 was set to a starting value of 0.5 kΩ and the reference value R_{bo} was set to 1550 Ω. The duty cycle sensitivity (*dc*-0.5)/($\Delta R_B/R_{bo}$) is about 0.276%/(mΩ/Ω) compared to an expected value of 0.253%/(mΩ/Ω), while the linearity error is smaller than ±0.6% of the span. The measurements were repeated by connecting the bridge to the circuit by means of a multipolar cable with a length of about 10 m, without observing significant variations.

Tests were carried out to evaluate the cross-sensitivity of duty cycle and frequency with respect to the bridge unbalance and overall bridge resistance, respectively. In Fig. 6 it can be observed that for a bridge unbalance variation of about ±2% with constant bridge resistance, the variation in the duty cycle is lower than 1.3%. In Fig. 7 it can be observed that for an overall bridge resistance variation of ±15%, the frequency variation is lower than 2 Hz.

The short-term frequency stability was evaluated by measuring the fluctuations in the output frequency at different values of the gate time τ set for the frequency counter. Fig. 8 shows the results where each point represents the frequency standard deviation σ measured over 200-sample populations as a function of the gate time.

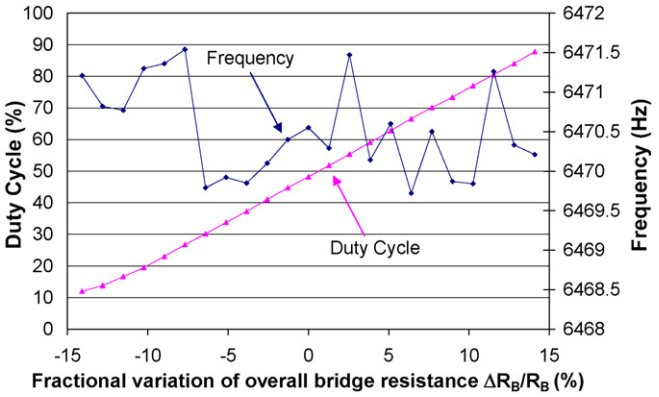


Fig. 7. Measured duty cycle and frequency vs. fractional variation of overall bridge resistance at constant bridge unbalance.

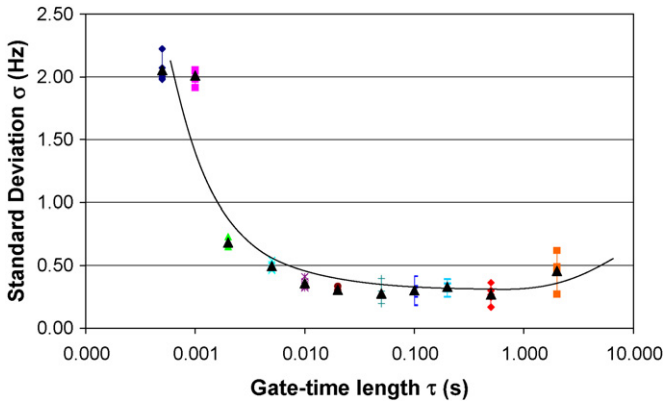


Fig. 8. Measured frequency S.D. vs. gate time length.

The behavior of the plot accounts for the contributions of random noise on the fluctuations of the output frequency *f*. The power spectral density $S(\nu)$ of the random noise of the signal frequency f can be expressed as a power sum of the Fourier frequency ν [14]. The standard deviation σ can be estimated by the following general relationship:

$$\sigma(\tau) = \sqrt{\int_{-\infty}^{+\infty} S(\nu)|H_\tau(\nu)|^2 \, \mathrm{d}\nu} \tag{3}$$

where $|H_\tau(\nu)|$ is the Fourier transform of the weight function associated with the gate time length τ. For short gate times, the white noise contribution (ν^0 term) is dominant, therefore by increasing the gate time the standard deviation is reduced. This trend proceeds until the flicker noise contribution (ν^{-1} term) becomes dominant, and the standard deviation tends to remain constant with the gate time. In our case, this occurs in the region between 20 and 200 ms, where the standard deviation is about 0.3 Hz. This value, taking into account the sensitivity, corresponds to a nominal resolution on the fractional bridge unbalance γ of about 5 ppm. For gate times longer than 1 s, the random-walk noise contribution (ν^{-2} term) becomes dominant and the standard deviation tends to increase with the gate time.

The effect of the sensitivity on the frequency stability was evaluated by repeating the measurements for different values of the gain-setting resistance R_G. Fig. 9 reports the obtained

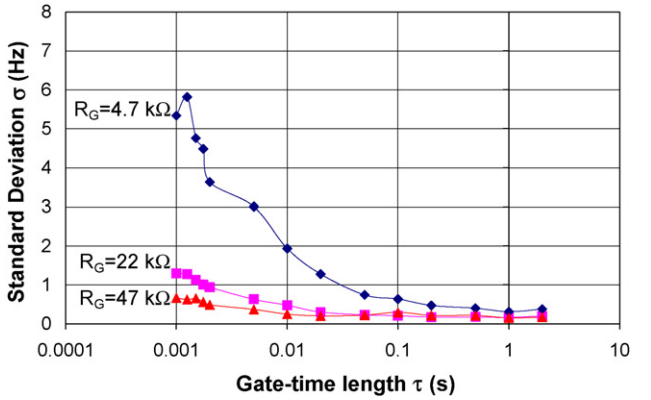


Fig. 9. Measured frequency standard deviation vs. gate-time length for different values of the gain resistor R_G.

results, showing that for gate times shorter than 100 ms the frequency stability worsens with increasing the sensitivity. On the other hand, for gate times beyond a few hundreds milliseconds, σ becomes constant. This implies that, with $R_G = 4.7\,k\Omega$ resulting in a sensitivity of 600 Hz/(1000 ppm), the circuit provides a resolution for γ better that 1 ppm at $\tau = 0.1$ s, i.e. at the rate of about 10 readings/s.

The main effects on the circuit performances related to the manufacturing technology nonidealities and deviations in the process parameters are the following. The first is the input offset voltage of the operational amplifiers whose maximum value is specified as 10 mV. However, the circuit architecture, thanks to the topology and the chopping action, is highly immune from offset related errors, as illustrated in Ref. [13]. Another aspect is the matching between polysilicon resistors. This was experimentally investigated by taking measurements on seven resistive test structures fabricated in the same technology used for the ASIC. The result was a measured matching between nominally identical resistors within 0.1% of the resistor value. Such a figure, which directly affects, for instance, the derivation of $V_{DD}/2$ from V_{DD}, determines a systematic error that is negligibly small [12,13].

4. Testing of the ASIC coupled to a SiC piezoresistive sensor

The circuit was interfaced to a piezoresistive silicon carbide (SiC) bridge sensor developed for high-temperature applications and intended to operate remotely from the electronic interface. The sensor, which is the unpackaged die intended to be used in a pressure transducer, consists of four 3-kΩ SiC piezoresistors deposited on a silicon diaphragm and connected in a full bridge configuration as shown in Fig. 10(a) and (b).

The sensor die was mounted on an alumina substrate that provides the mechanical support and carries the electrical connections. The sensor can be heated by means of a resistive heater realized in thick-film technology on alumina and attached to the bottom face of the sensor substrate. The sensor–heater stack, shown in Fig. 11, was mounted in a dedicated test system, which allows the application of known microdeformations to the sensor

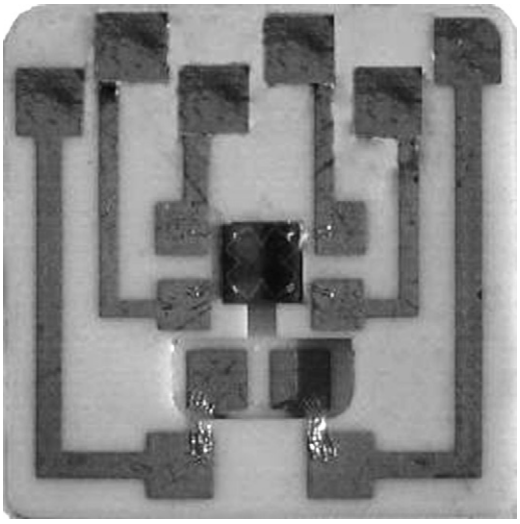


Fig. 11. SiC sensor and heating element in thick-film technology on alumina substrate.

at different temperatures. The setting of the sensor temperature is obtained by means of a feedback control system based on the pyrometric reading of the temperature and the adjustment of the electrical power supplied to the heater [15]. The sensor only was subject to temperature variations, while the ASIC was connected and kept at a distance maintained at room temperature. The current-mode driving of the bridge avoided accuracy degradation for the remotely placed sensor.

The external components were set to the following values: $C_0 = 2.2$ nF, $R_{ref} = 67.8\,k\Omega$, $R_G = 47\,k\Omega$, $R_{bo} = 3.1\,k\Omega$.

The fractional bridge unbalance and the circuit output frequency were measured simultaneously and independently as a function of the applied load at room temperature. Fig. 12 shows the frequency versus the fractional bridge unbalance. The frequency sensitivity is 170.3 Hz/(1000 ppm) in good agreement with the theoretical sensitivity of 171 Hz/(1000 ppm). The best-fit line nonlinearity results smaller than ±0.2% of the span.

The overall bridge resistance and the duty cycle of the output signal were measured simultaneously and independently as a function of the sensor temperature for the unloaded bridge.

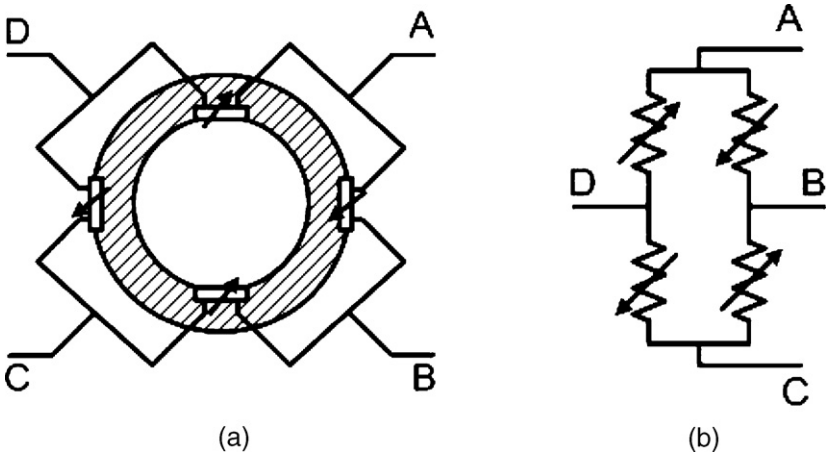


Fig. 10. Structure of the SiC piezoresistive sensor (a); piezoresistor connections (b).

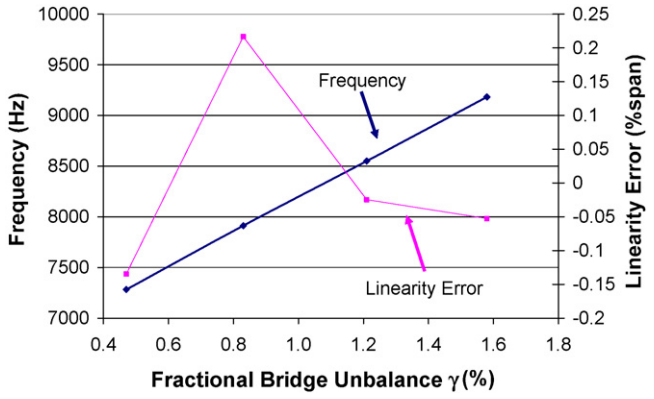


Fig. 12. Measured output frequency vs. fractional unbalance.

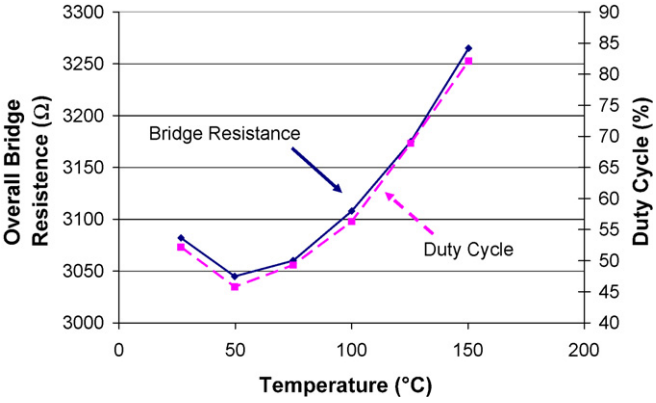


Fig. 13. Measured overall bridge resistance and output duty cycle as a function of temperature.

Fig. 13 shows the results where the duty cycle follows the bridge resistance behavior as expected. It can be observed that the temperature coefficient of resistance (TCR) changes sign at around 50 °C. Fig. 14 shows the duty cycle plotted versus the fractional variation of the overall bridge resistance. The trend is linear and the measured sensitivity results 0.51%/(mΩ/Ω) in good agreement with the expected value of 0.47%/(mΩ/Ω).

The measurements of the fractional bridge unbalance γ and of the circuit output frequency f as a function of the applied load have been repeated at different sensor temperatures, after setting the output duty cycle to about 50% at room temperature. The resulting fractional bridge unbalance-versus-load sensitivity S_γ and frequency-versus-load sensitivity S_f as a function of the temperature are shown in Figs. 15 and 16, respectively. In the temperature range between 75 and 150 °C, the sensitivity S_f tends to be constant. This is due to the positive TCR of the bridge resistance R_B, shown in Fig. 14, and the negative slope of the sensitivity S_γ shown in Fig. 15, that favourably combine with the current excitation of the bridge to provide first-order thermal compensation [13].

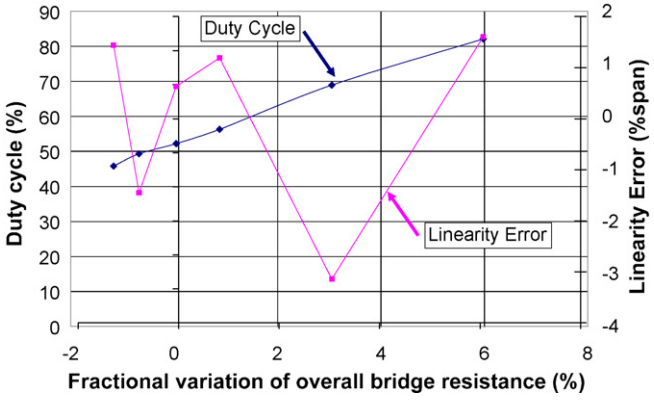


Fig. 14. Measured duty cycle vs. fractional variation of overall bridge resistance.

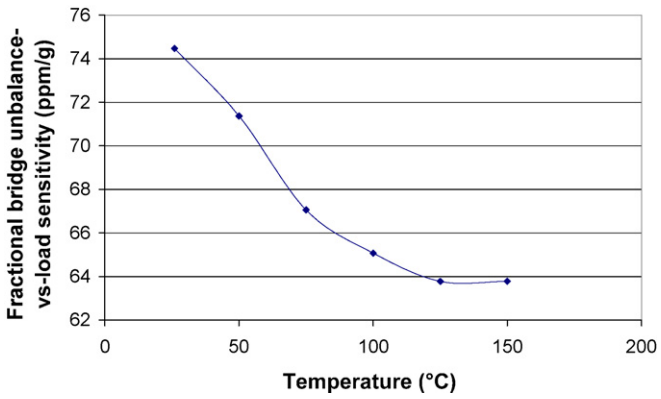


Fig. 15. Fractional bridge unbalance-vs.-load sensitivity as a function of temperature.

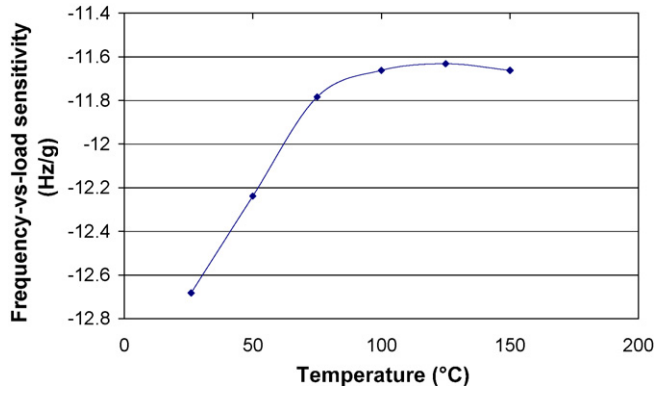


Fig. 16. Frequency-vs.-load sensitivity as a function of temperature.

5. Conclusions

An ASIC interface for resistive-bridge sensors based on a relaxation oscillator has been designed, manufactured and characterized. The output frequency and duty cycle are proportional to the unbalance and the overall resistance of the sensor bridge, respectively. Therefore, the circuit allows the additional measurement of the sensor temperature and sends its value on the same signal used for the bridge unbalance with no cable extra-cost. The quasi-digital nature of the output increases the noise immunity and simplifies the interfacing to digital systems. The constant-current bridge excitation is suited for remotely placed sensors without suffering accuracy degradation and gives a first-order thermal compensation with piezoresistive semiconductor sensors.

The interface has been tested with a reference bridge. The experimental results are in agreement with the theoretical predictions. Cross-sensitivity measurements have shown a negligible correlation between frequency and duty cycle.

The circuit has been coupled to a piezoresistive SiC bridge sensor for high-temperature applications and tested with a dedicated measuring system. Results have shown a behavior in agreement with expectations, with a degree of thermal compensation provided in the temperature range 75–150 °C where the sensor thermal coefficient of sensitivity and TCR have opposite signs.

References

[1] N.M. Mohan, V.J. Kumar, A novel signal conditioning circuit for push–pull-type resistive transducers, Meas. Sci. Technol. 16 (2005) 1848–1852.

[2] J. Zhang, A. Mason, Characterization of a configurable sensor signal conditioning circuit for multi-sensor microsystems, in: Proceedings of the IEEE Sensors, Vienna, October 24–27, 2004, pp. 198–201.

[3] C. Falconi, C. Di Natale, A. D'Amico, M. Faccio, Electronic interface for the accurate read-out of resistive sensors in low voltage–low power integrated systems, Sens. Actuators A 117 (1) (2005) 121–126.

[4] S. Vlassis, S. Siskos, A signal conditioning for piezoresistive pressure sensors with variable pulse-rate output, Analog Integr. Circ. Signal Proc. 23 (2000) 153–162.

[5] S. Kaliyugavaradan, A simple resistance-to-time converter for signal conditioning of resistive transducers, Meas. Sci. Technol. 11 (2000) N73–N75.

[6] F. Van Goes, G. Meijer, A universal transducer interface for capacitive and resistive sensor elements, Analog Integr. Circ. Signal Proc. 14 (1997) 249–260.

[7] K. Mochizuki, K. Watanabe, A linear resistance-to-frequency converter, in: Proceedings of the IMTC, Waltham, 1995, pp. 339–343.

[8] J.H. Huijsing, G.A. Van Rossum, M. Van der Lee, Two-wire bridge-to-frequency converter, IEEE J. Solid-State Circ. SC-22 (3) (1987) 343–349.

[9] N.V. Kirianaki, S.Y. Yurish, N.O. Shpak, V.P. Deynega, Data Acquisition and Signal Processing for Smart Sensors, 1st ed., John Wiley & Sons, Chichester, 2002.

[10] F. Reverter, M. Gasulla, R. Pallas-Areny, Analysis of power supply interference effects on quasi-digital sensors, Sens. Actuators A 119 (1) (2005) 187–195.

[11] S.Y. Yurish, N.V. Kirianaki, R. Pallàs-Areny, Universal frequency-to-digital converter for quasi-digital and smart sensors: specification and applications, Sens. Rev. 25 (2) (2005) 92–99.

[12] V. Ferrari, C. Ghidini, D. Marioli, A. Taroni, Oscillator-based signal conditioning with improved linearity for resistive sensors, IEEE Trans. Instrum. Meas. 47 (1) (1998) 293–298.

[13] V. Ferrari, D. Marioli, A. Taroni, Oscillator-based interface for measurand-plus-temperature readout from resistive bridge sensors, IEEE Trans. Instrum. Meas. 49 (3) (2000) 585–590.

[14] J. Rutman, F.L. Walls, Characterization of frequency stability in precision frequency sources, Proc. IEEE 79 (7) (1991) 952–960.

[15] D. Crescini, M. Romani, D. Marioli, A. Taroni, Development of a test structure for the characterization of piezoresistive films in SiC, in: Proceedings of the SENSOR 2005, Nuremberg, May 10–12, 2005, pp. 511–515.

Biographies

Vittorio Ferrari was born in Milan, Italy, in 1962. In 1988 he obtained the laurea degree in physics *cum laude* at the University of Milan. In 1993 he received the research doctorate degree in electronic instrumentation at the University of Brescia. From 1993 to 2005 he was an assistant professor and an associate professor, and since 2006 he has been a full professor of electronics at the Faculty of Engineering of the University of Brescia. His research activity is in the field of sensors and the related signal-conditioning electronics. Topics of interest are acoustic-wave piezoelectric sensors, microresonant sensors and MEMS, autonomous sensors and energy harvesting, oscillators for resonant sensors and frequency-output interface circuits. He is currently involved in national and international research programmes on piezoelectric transducers and resonant sensor systems, and in projects in cooperation with industries.

Alessio Ghisla was born in Brescia, Italy, in 1972. In 2001, he received the laurea degree in electronic engineering from the Faculty of Engineering, University of Brescia, Brescia, Italy. From September 2001 to October 2002 he has been collaborating with the Department of Electronics and Automation, University of Brescia. In 2006 he received the research doctorate degree in electronic instrumentation from the University of Brescia, Italy. His main research interests are the design and characterization of sensors and of the electronic interfaces for sensors, with particular regard to capacitive sensors for position measurement and MEMS sensors.

Zsolt M. Kovacs Vajna was born in Budapest (Hungary) in 1963. He received the DEng degree with honors from the University of Bologna, Italy, in 1988 and the PhD degree in "electronics engineering and computer sciences" from the same University in 1994. From 1989 to 1998 he was with the Department of Electronics Engineering (DEIS) in Bologna, where he was assistant professor and research associate in electronics. In 1998 he joined the Department of Electronics Engineering (DEA) of the University of Brescia, Italy. He is currently full professor of electronics and teaches the courses of "microelectronics" and "electronics circuit design". His research activities covered circuit simulation techniques, electromagnetic interference analysis in integrated circuits, several aspects of pattern recognition and integrated voltage converters based on capacitors or on inductors. Currently he is involved in integrated circuit design for innovative applications and technologies, as for example, integrated UWB radars for civil applications. He authors more than 100 international scientific publications, including articles in journals, in conference proceedings and 16 international patents. He is senior member of the IEEE.

Daniele Marioli was born in Brescia, Italy, in 1946. He obtained the electrical engineering degree in 1969. From 1984 to 1989 he was an associate professor in applied electronics and since 1989 he has been a full professor of electronics at the University of Brescia. His main field of activity is the design and experimentation of analog electronic circuits for the processing of electrical signals from transducers, with particular regard to S/N ratio optimization.

Andrea Taroni was born in 1942. He received the degree in physical science from the University of Bologna, Italy, in 1966. He was an associate professor at the University of Modena from 1971 to 1986. Since 1986 he has been full professor of electrical measurements at the University of Brescia. He has done extensive research in the field of sensors for physical quantities and electronic instrumentation, both developing original devices and practical applications. He is author of more than 100 scientific papers.